**Instruction Code**

**Stored Program Organization**

The simplest way to organize a computer

* One processor register: AC (accumulator)
  + The operation is performed with the memory operand and the content of AC.
* Instruction code format with two parts: Opcode and Address
  + Opcode: specify 16 possible operations (4-bit)
  + Address: specify the address of an operand (12-bit)
  + If an operation in an instruction code does not need an operand from memory, the rest of the bits in the instruction (Address field) can be used for other purpose.
* Memory: 12-bit = 4096 location = 4096 word (instruction and data are stored)
  + Store each instruction code (program) and operand (data) in 16-bit memory word.
* **Addressing Mode:**
  + Immediate operand address (Immediate Addressing mode)
    1. The second part of instruction code (address field) specifies operand.
  + Direct operand address (Direct Addressing mode)
    1. The second part of instruction code specifies the address of operand. (i.e. the given address is effective address).
  + Indirect operand address (Indirect Addressing mode)
    1. The bits in the second part of the instruction designate an address of a memory word in which the address of the operand is found (pointer).
  + One bit of the instruction code is used to distinguish between direct and indirect address.
  + Effective address: Address where an operand is physically located.
* **Direct Address**
  + Occurs when the operand part contains the address of needed data.
    1. Address part of IR (Instruction Register) is placed on the bus and loaded back into the AR (Address Register).
    2. Address is selected in memory and its data placed on the bus to be loaded into the data register (DR) to be used for requested instruction.
* **Indirect Address**
  + Occurs when the operand contains the address of the address of needed data.
    1. Address part of IR is placed on the bus and loaded back into the AR.
    2. Address is selected in memory and placed on the bus to be loaded back into the AR.
    3. New address is selected in memory and placed on the bus to be loaded into the DR to use later.
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